LOW-DIMENSIONAL SURFACE NANOSTRUCTURES STUDIED BY SCANNING TUNNELING MICROSCOPY

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With a further miniaturization of functional devices for information technology, novel nanoprobe technology for fabrication, manipulation and characterization of low-dimensional surface nanostructures with atomic-scale resolution has been highly required. Such a novel nanometer-scale processing tool with multiple functions plays an important role in the interdisciplinary research on materials nano-architectonics. Here our recent achievements in the application of scanning tunneling microscopy and spectroscopy (STM/STS) to atomic-scale fabrication, manipulation and characterization in ultrahigh vacuum (UHV) and at low temperatures (LT) are presented.

Firstly, exploration of the true ground state and the reversible phase manipulation on Si(001) reconstructed surfaces will be discussed using high resolution LT-UHV STM/STS. Although the Si(001) wafer has been the most important substrate material in semiconductor industry and nano-electronics, and its surface has been extensively and intensively studied for decades, the ground state of Si(001) surface at LT, having the most stable atomic-configuration, has been a matter of controversy in surface physics for the decade [2]. As schematically shown in Fig.1, there have been various papers reporting the observation of different surface structures for the ground state of Si(001) surfaces (static (2×1), dynamic (2×1), c(4×2) and p(2×2)) using various surface analysis methods such as LT-STM, LT noncontact-AFM and LT-LEED. It should be noted that the reconstruction on Si(001) surfaces involve dimerization, which creates the unique one-dimensional property of this surface. The dimerization removes one of the two dangling bonds (DB) associated to each atom on the bulk terminated surfaces. Further reconstruction can be characterized by dimer buckling, opening up an energy gap between the two remaining DBs. As a result, the remaining DBs form filled and empty states at the Si(001) surface.

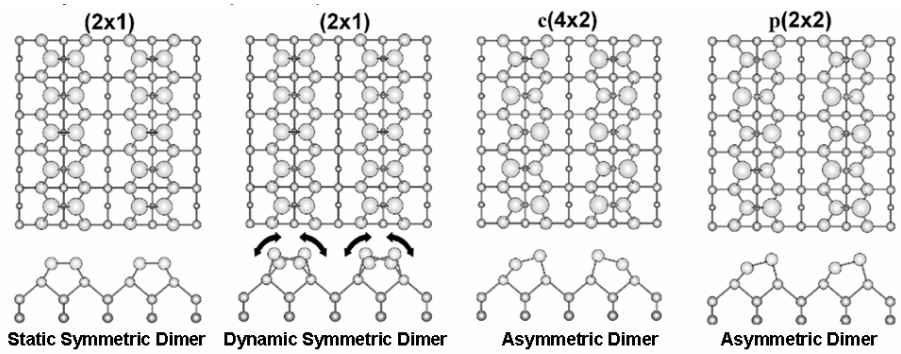

Fig. 1. The proposed atomic configurations on Si(001) at low temperatures (< 50K).

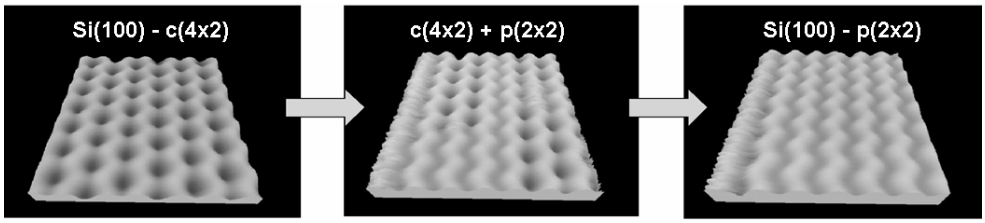

Fig. 2 Reversible phase manipulation between the ground state c(4×2) and quasi-ground state p(2×2).

Our LT-STM analysis has discarded the (2×1) cases first. Furthermore, it has clarified that the emergence of p(2×2) and the flip-flop dimers at LT is generated by an STM scan at a specific bias voltage, and is not the intrinsic nature of the Si(001) surface [2]. The injection of tunneling electrons or holes into a particular surface state plays an important role in the surface phase modification. Finally we have discovered how to manipulate the surface phases between c(4×2) and p(2×2) by controlling the tunneling conditions (Fig.2). From such findings, we concluded that the ground state of Si(001) is c(4×2) phase [3].

The empty DB state, which is located in the bulk band gap, reveals dispersive in the direction of the dimer row, and may be regarded as one-dimensional (1D) electronic state. LT-STM/STS observations clearly show a 1D electronic characteristic along the dimer row [4]. Taking advantage of STM atom manipulation, we have succeeded in the fabrication of an artificial 1D quantum well on a single Si dimer row by depositing tungsten atom dots from STM tips [5]. The energy-resolved imaging (*dI/dV*) shows wave patterns of different amplitudes and oscillation periods as the sample bias is varied. These results clarify that the DB state is confined between the artificial potential barriers and it behaves as a 1D quantum well (QW). The observed differential conductance (LDOS) images in Fig.3 shows that 1D confinement in the artificial QW can be explained by a parabolic potential well. These results clearly prove that the atomic scale 1D electronic states can be artificially fabricated and analyzed by high resolution LT-STM/STS techniques.

Finally, recent new findings on the artificial atomic structure fabricated on Si(111)-(7×7) surfaces at LT will be presented.

Based on the combination of STM nano-processing capability and advanced physical fields, we expect to promote the novel nanomaterials research by the nano-architectonics principle.

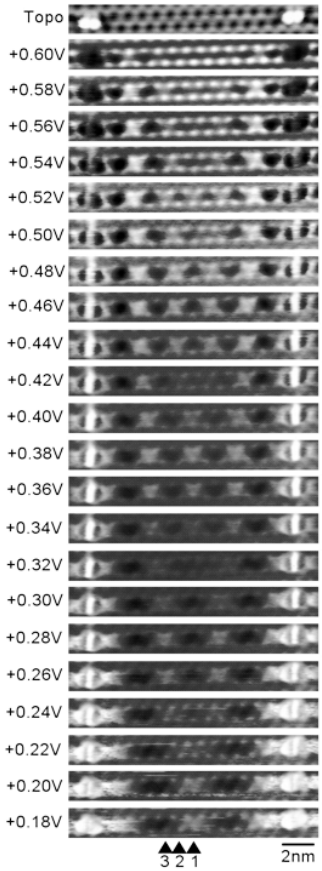

Fig. 3 Top: STM topography image of QW fabricated on a single Si(001) dimer row.
Others: Differential conductance (*dI/dV*) images for various sample bias voltages.

Acknowledgements

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References

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